What is a Logic Block?
An Introduction to the Basis of FPGA Architectures

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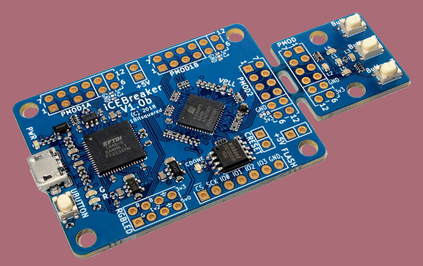
What is an FPGA?

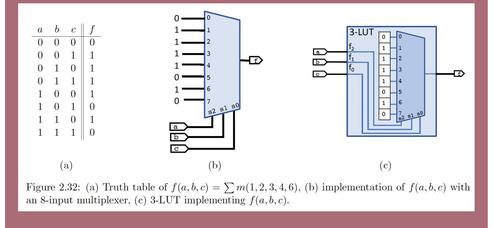
- Field Programmable Gate Array
- Integrated Circuit
- Implement logic circuits outside fab
- Use hardware description language to create a logic circuit
- Applications: motor control, machine vision, medical devices



iCEBreaker FPGA Development Board
FPGA: Lattice iCE40UP5k

Look Up Tables

- Table of inputs mapped to outputs
- Implemented as a 2^n input mux, inputs are the selectors, values are preloaded by compiler
- Act as a truth tables
- Can be cascaded with other LUTs to create wider functions



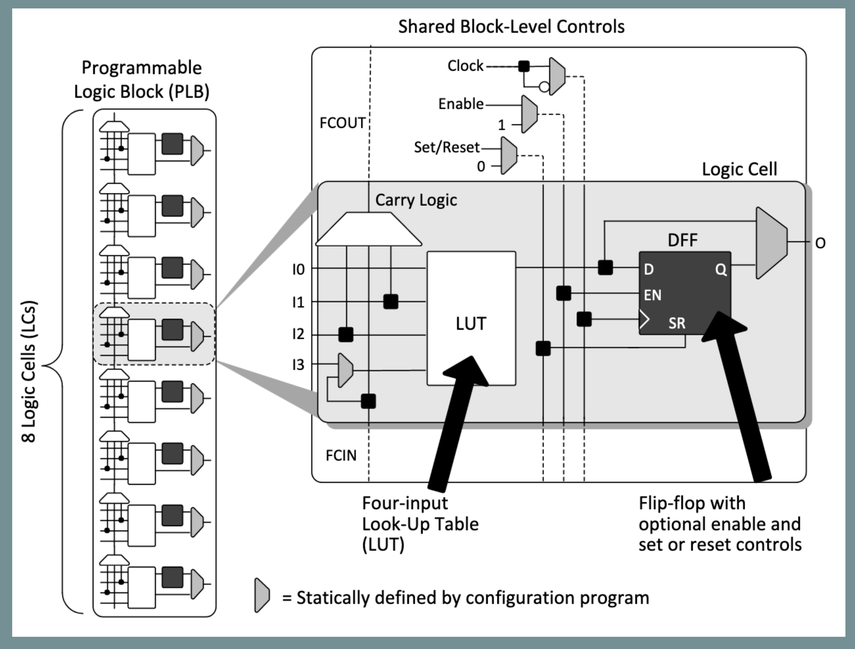
a	b	c	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(a) (b) (c)

Figure 2.32: (a) Truth table of $f(a,b,c) = \sum m(1,2,3,4,6)$, (b) implementation of $f(a,b,c)$ with an 8-input multiplexer, (c) 3-LUT implementing $f(a,b,c)$.

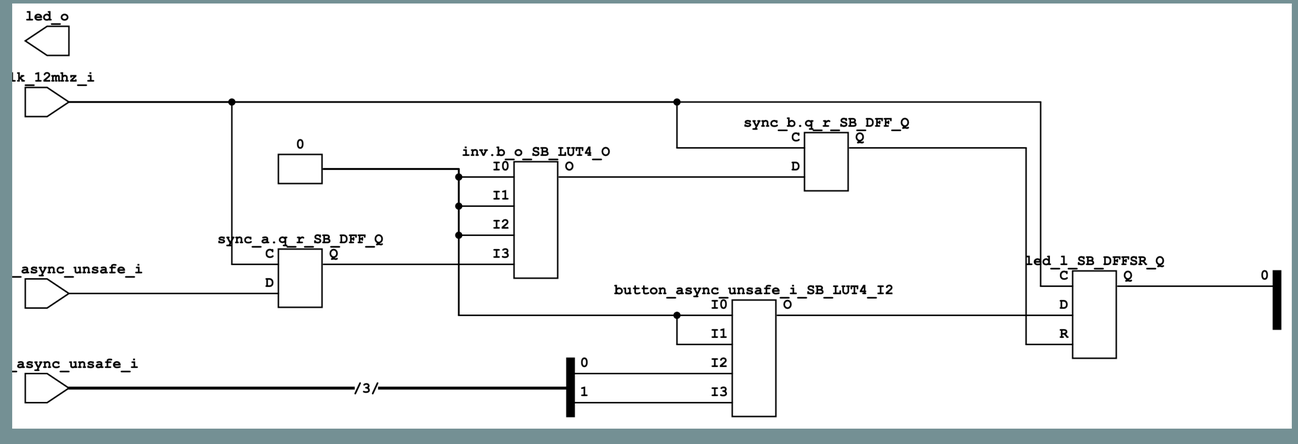
Look Up Table Implementation
-Beginning Logic Design by Martine Schlag (CSE 100 Textbook)

Logic Block Diagram and Synthesized Circuit Example



(Left) Logic Block Diagram for the Lattice iCE40UP5k datasheet.
Uses 4 input LUTs with carry logic to optimize arithmetic logic such as adding.
D flip flops have 4 inputs for data in, clock, clock enable, and set/reset.
Can bypass D flip flop if combinational logic output is desired with use of mux.

(Bottom) Yosys synthesized circuit of a 2 input AND gate ran through a D flip flop with synchronous reset.
Can you find where the LUTs and D flip flops are?
Can you trace the circuit below?



D Flip Flops

- Basic storage element
- Needs a clock signal to synchronize
- Capable of feedback logic
- Required for synchronous circuits
- Examples of synchronous circuits: multipliers, counters, edge detectors

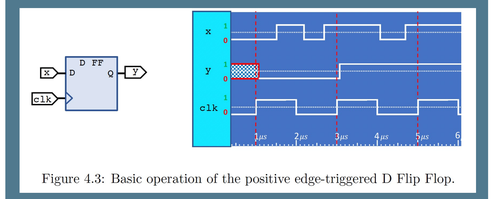


Figure 4.3: Basic operation of the positive edge-triggered D Flip Flop.

D Flip Flop Operation and Timing
-Beginning Logic Design by Martine Schlag (CSE 100 Textbook)

Overview

Lookup tables contain the logic values for logic functions
D flip flops use clocks to synchronize logic
With the two, FPGAs can create both combinational and synchronous logic circuits

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