310-981-7473
Los Angeles
gerardomejiamtz117@gmail.com

Gerardo (Gary) Mejia Martinez

GitHub: gmejiamtz
LinkedIn: gmejiamtz

Education

Bachelor of Science: Computer Engineering **Sept 2020 - June 2024**
University of California, Santa Cruz *GPA: 3.51*

Main courses: Computer Architecture(Graduate), Computer Systems and C Programming, Embedded System Design, Logic Design(Graduate), VLSI Digital System Design(Graduate), Open Source Hardware Design

Work Experience

Peer Tutor **Jan 2022 - Present**
University of California, Santa Cruz *Santa Cruz, CA*

- Tutored Introduction to Logic Design and VLSI Digital System Design.
- Created an install guide to install VLSI tools natively on Apple Silicon from source.
- Taught students how to read and create basic Verilog testbenches to debug Vivado FPGA projects
- Learned to how to identify problems in other's work and communicate suggestions to find solutions.

Tooling Engineering Intern **Feb 2021 - May 2021 | July 2023 - Sept 2023**
Marvin Engineering Company *Inglewood, CA*

- Gained hands on workshop skills required for industrial machining and mass manufacturing problems.
- Developed thinking process required to produce efficient solutions in manufacturing engineering.
- Produced industrial standard engineering drawings and CAD models to prototype custom tooling for aerospace manufacturing applications
- Learned to make mistakes in a professional environment and find a proper and timely solution.

Projects

BOOM2 Bubble Sort Optimized CPU **Nov 2023**
Graduate Computer Architecture Final Project

- Used ESESC, a UCSC RISCV CPU simulator, to simulate a BOOM2 CPU running a bubble sort of 2147483647 integers in the worst case
- Created a Bash script to set up ESESC test benches to run the workload and store all outputted data into a unique directory
- Found the bottle neck to be L2 having a 100% miss rate thus doubled block size from 32 to 64 and halved associativity from 16 to 8 to get 1.5x IPC increase

Read Only Memory Verilog Model **May 2023**
Open Source Contribution to OpenRAM

- Used Python to create a Verilog behavioral model to describe a ROM for OpenRAM, a memory compiler
- Goal of the model is to be used in a Verilog testbench to verify ROM initializes and reads correctly
- Verified ROM function using a Verilog testbench with iVerilog to create a waveform to display in GTKWave
- Learned how to use Git to track changes for review, pass regression tests, and feature deployment

Space Invaders **Mar 2023**
Logic Design with Verilog - Final Project

- Used an Icebreaker development board with an iCE40UP5k FPGA to make a Space Invaders like shooting game using SystemVerilog
- Goal of the game is to shoot and hit the moving enemy block before it reaches the player's level. Enemy moves faster each time it touches the edge of the screen
- Designed four state machines to control player movement, enemy movement, bullet collision and display
- Learned how to create a Verilog testbench to simulate state machines using iVerilog and GTKWave to display waveforms

Skills

Programming	Bash, C/C++, Matlab, Python, Rust
Hardware Design	iVerilog, OpenLane, pyMTL, Verilog/SystemVerilog, Vivado, Yosys
Other	GDB, Git, LaTeX, Valgrind, ESP-IDF